

## 200-V Half-Bridge Driver With Shutdown Input

### Features

- Gate drive supplies up to 20 V per channel
- Under voltage lockout for  $V_{CC}$ ,  $V_{BS}$
- 3.3 V, 5 V, 15 V input logic compatible
- Tolerant to negative transient voltage
- Designed for use with bootstrap power supplies
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set dead time
- High-side output in phase with input
- Shutdown input turns off both channels
- -40 °C to 125 °C operating range
- RoHS compliant

### Description

The IRS2008S is a high voltage, high speed power MOSFET driver with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 V. Propagation delays are matched to simplify the HVIC's use in high frequency applications.

### Product Summary

$V_{\text{OFFSET}}$	$\leq 200 \text{ V}$
$V_{\text{OUT}}$	10 V – 20 V
$I_{\text{O+}} \& I_{\text{O-}}$ (typ.)	290 mA & 600 mA
$t_{\text{ON}} \& t_{\text{OFF}}$ (typ.)	680 ns & 150 ns
Deadtime (typ.)	520 ns

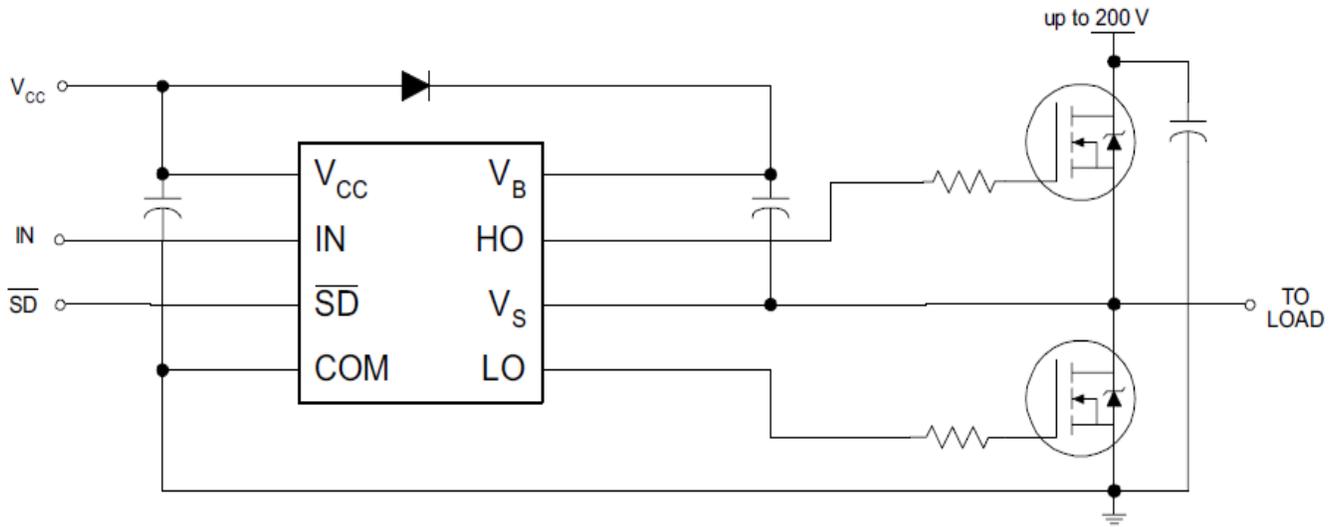
### Package Options



### Typical Applications

- Appliance motor drives
- Servo drives
- Micro inverter drives
- General purpose three phase inverters

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRS2008SPBF	8-Lead SOIC	Tube/Bulk	95	IRS2008SPBF
		Tape and Reel	2500	IRS2008STRPBF

**Typical Connection Diagram**


(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer our Application Notes & DesignTips for proper circuit board layout.

### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
$V_{CC}$	Low side supply voltage	-0.3	25 <sup>†</sup>	V	
$V_{IN}$	Logic input voltage (IN & $\overline{SD}$ )	COM - 0.3	$V_{CC} + 0.3$		
$V_B$	High-side floating well supply voltage	-0.3	225		
$V_S$	High-side floating well supply return voltage	$V_B - 25$	$V_B + 0.3$		
$V_{HO}$	Floating gate drive output voltage	$V_S - 0.3$	$V_B + 0.3$		
$V_{LO}$	Low-side output voltage	COM - 0.3	$V_{CC} + 0.3$		
COM	Power ground	$V_{CC} - 25$	$V_{CC} + 0.3$		
$dV_S/dt$	Allowable $V_S$ offset supply transient relative to COM	—	50	V/ns	
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	8-Lead SOIC	—	0.625	W
$R_{thJA}$	Thermal resistance, junction to ambient	8-Lead SOIC	—	200	$^\circ\text{C/W}$
$T_J$	Junction temperature	—	150	$^\circ\text{C}$	
$T_S$	Storage temperature	-55	150		
$T_L$	Lead temperature (soldering, 10 seconds)	—	300		

† All supplies are tested at 25V

### Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of  $(V_{CC} - COM) = (V_B - V_S) = 15\text{ V}$ .

Symbol	Definition	Min	Max	Units
$V_{CC}$	Low-side supply voltage	10	20	V
$V_{IN}$	Logic input voltage(IN & $\overline{SD}$ )	0	$V_{CC}$	
$V_B$	High-side floating well supply voltage	$V_S + 10$	$V_S + 20$	
$V_S$	High-side floating well supply offset voltage <sup>†</sup>	COM - 8 <sup>†</sup>	200	
$V_{HO}$	Floating gate drive output voltage	$V_S$	$V_B$	
$V_{LO}$	Low-side output voltage	COM	$V_{CC}$	
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

† Logic operation for  $V_S$  of  $-8\text{ V}$  to  $200\text{ V}$ . Logic state held for  $V_S$  of  $-8\text{ V}$  to  $-V_{BS}$ . Please refer to Design Tip DT97-3 for more details.

### Static Electrical Characteristics

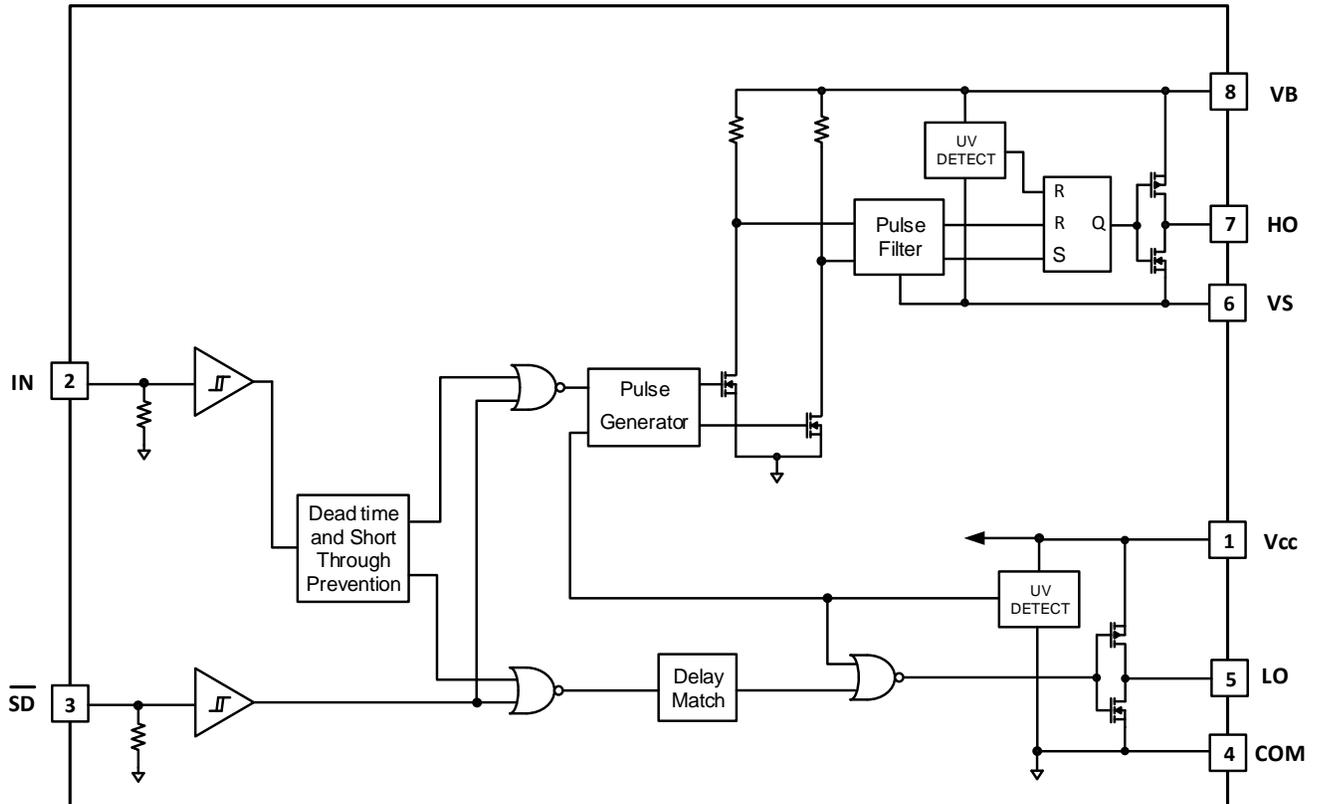
$(V_{CC} - COM) = (V_B - V_S) = 15\text{ V}$ .  $T_A = 25\text{ }^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to respective  $V_S$  and COM and are applicable to the respective output leads HO or LO. The  $V_{CCUV}$  parameters are referenced to COM. The  $V_{BSUV}$  parameters are referenced to  $V_S$ .

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{BSUV+}$	$V_{BS}$ supply under voltage positive threshold	8.0	8.9	9.8	V	
$V_{BSUV-}$	$V_{BS}$ supply under voltage negative threshold	7.4	8.2	9		
$V_{BSUVHY}$	$V_{BS}$ supply under voltage hysteresis	—	0.7	—		
$V_{CCUV+}$	$V_{CC}$ supply under voltage positive threshold	8.0	8.9	9.8		
$V_{CCUV-}$	$V_{CC}$ supply under voltage negative threshold	7.4	8.2	9		
$V_{CCUVHY}$	$V_{CC}$ supply under voltage hysteresis	—	0.7	—		
$I_{LK}$	High-side floating well offset supply leakage	—	—	50	$\mu\text{A}$	$V_B = V_S = 200\text{ V}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	45	75		All inputs are in the off state
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	300	520		
$V_{OH}$	High level output voltage drop, $V_{BIAS} - V_O$	—	0.05	0.2	V	$I_O = 2\text{ mA}$
$V_{OL}$	Low level output voltage drop, $V_O$	—	0.02	0.1		
$I_{O+}$	Output high short circuit pulsed current	200	290	—	mA	$V_O = 0\text{ V}$ $PW \leq 10\text{ }\mu\text{s}$
$I_{O-}$	Output low short circuit pulsed current	420	600	—		$V_O = 15\text{ V}$ $PW \leq 10\text{ }\mu\text{s}$
$V_{IH}$	Logic "1" (HO) & Logic "0" (LO) input voltage	2.5	—	—	V	$V_{CC} = 10\text{ V} - 20\text{ V}$
$V_{IL}$	Logic "0" (HO) & Logic "1" (LO) input voltage	—	—	0.8		
$V_{SD,TH+}$	SD input positive going threshold	2.5	—	—		
$V_{SD,TH-}$	SD input negative going threshold	—	—	0.8		
$I_{IN+}$	Logic "1" Input bias current	—	3	10	$\mu\text{A}$	$V_{IN} = 5\text{ V}$
$I_{IN-}$	Logic "0" Input bias current	—	—	5		$V_{IN} = 0\text{ V}$

### Dynamic Electrical Characteristics

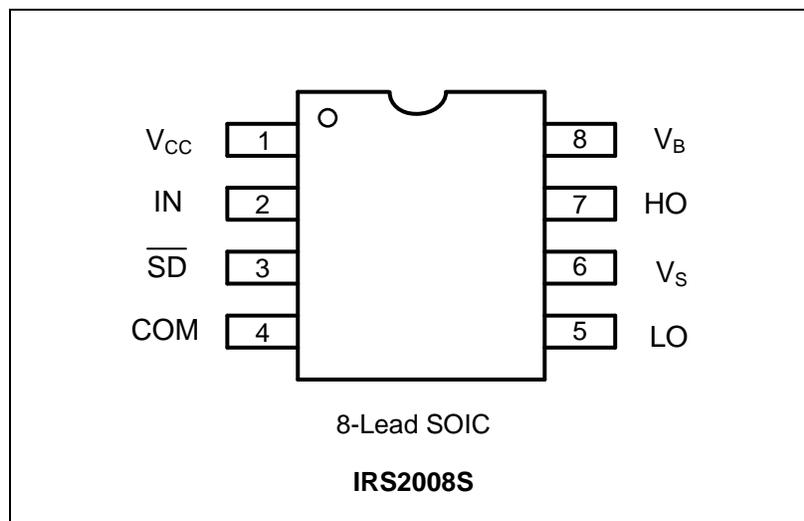
$V_{CC} = V_B = 15\text{ V}$ ,  $V_S = \text{COM}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , and  $C_L = 1000\text{ pF}$  unless otherwise specified.

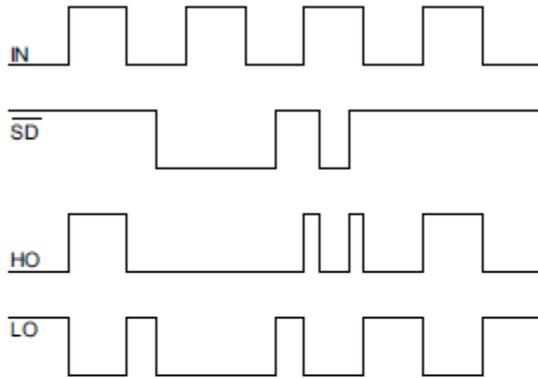
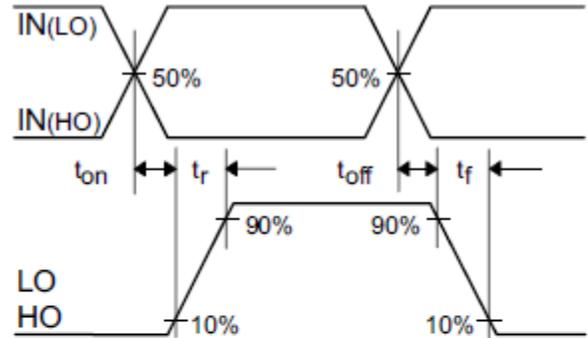
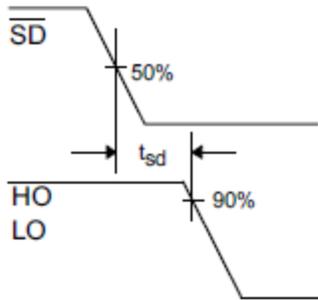
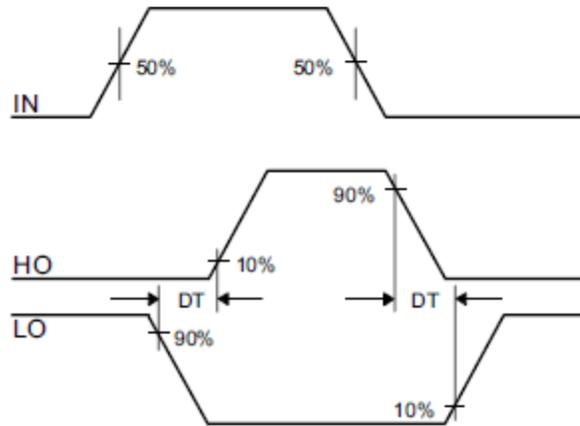
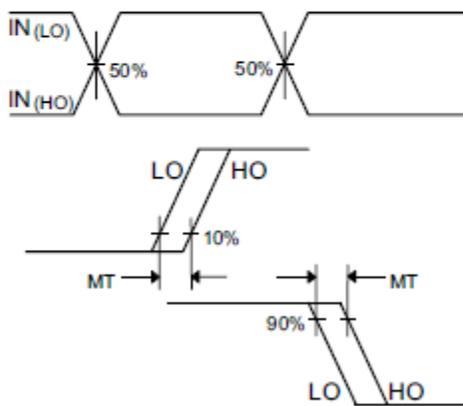
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{ON}$	Turn-on propagation delay	—	680	870	ns	$V_S = 0\text{ V}$ or $200\text{ V}$
$t_{OFF}$	Turn-off propagation delay	—	150	220		
$t_{SD}$	Shutdown propagation delay	—	160	220		
$t_R$	Turn-on rise time	—	70	170		$V_S = 0\text{ V}$
$t_F$	Turn-off fall time	—	30	90		
DT	Dead time, LO turn-off to HO turn-on & HO turn-off to LO turn-on	400	520	650		
MT	Delay matching time ( $t_{ON}$ , $t_{OFF}$ )	—	—	60		

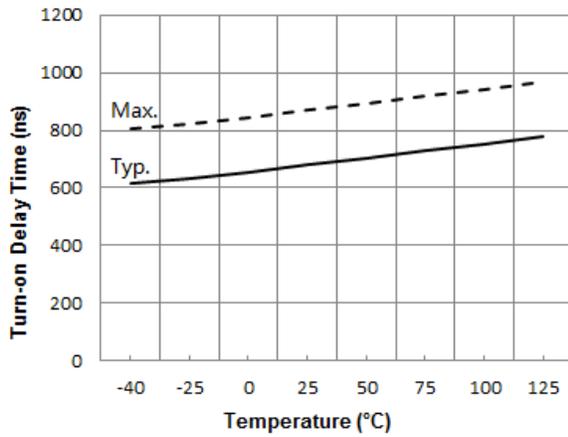
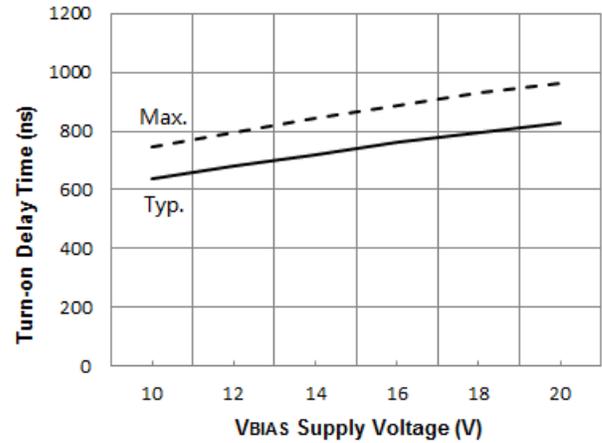
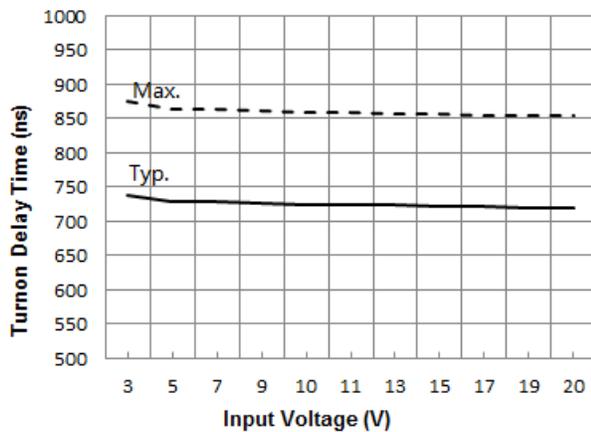
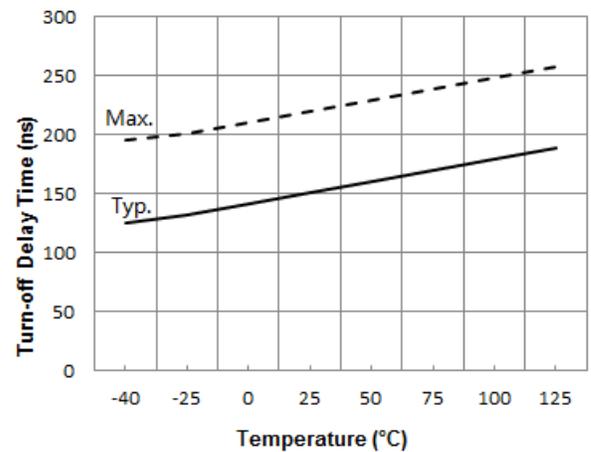
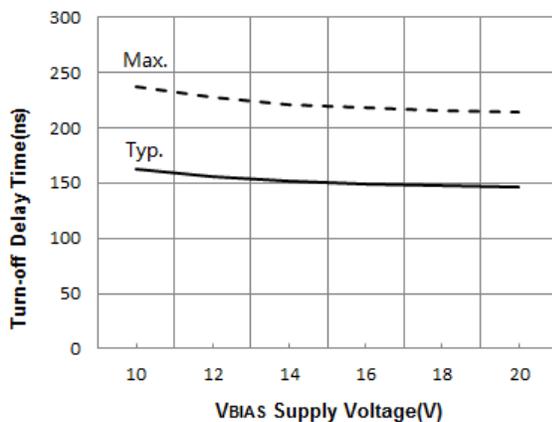
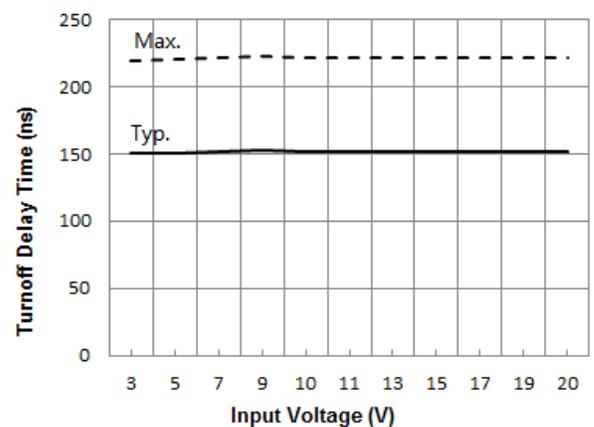
**Functional Block Diagram**


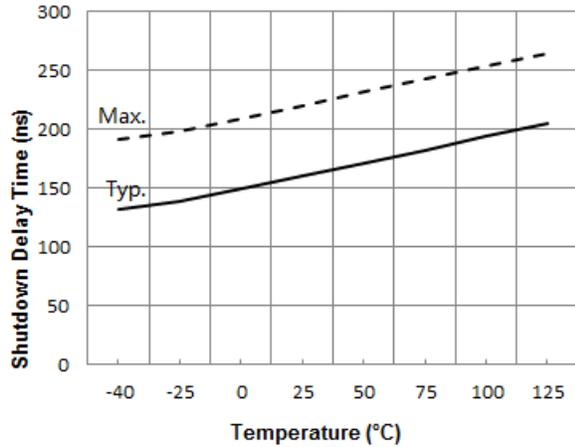
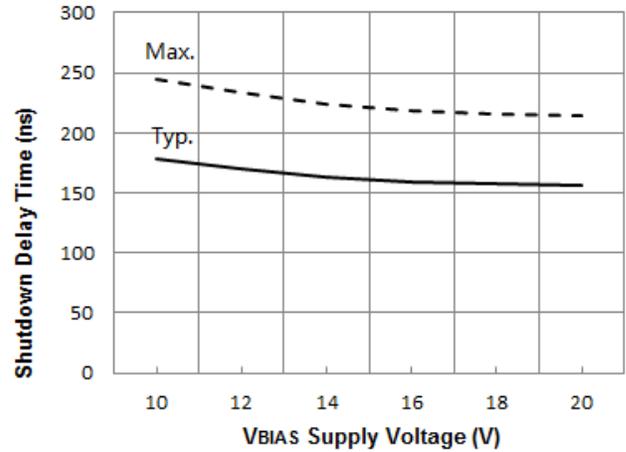
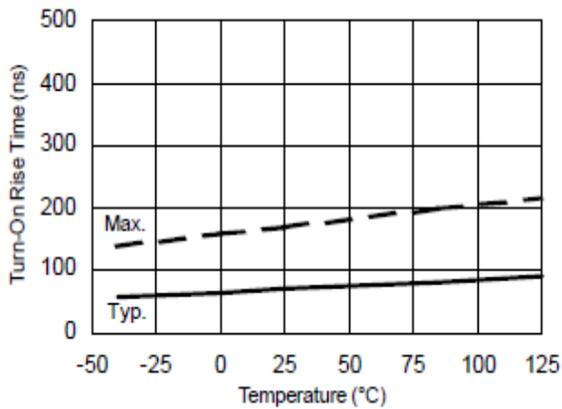
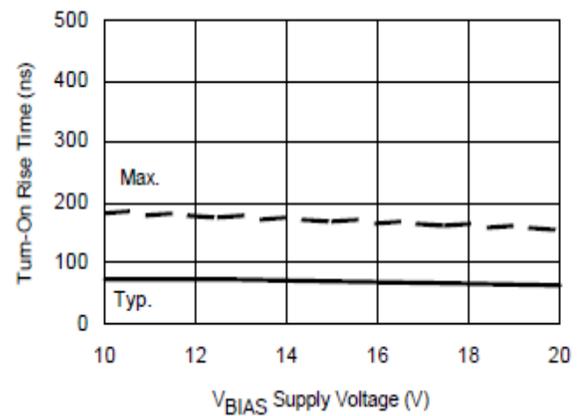
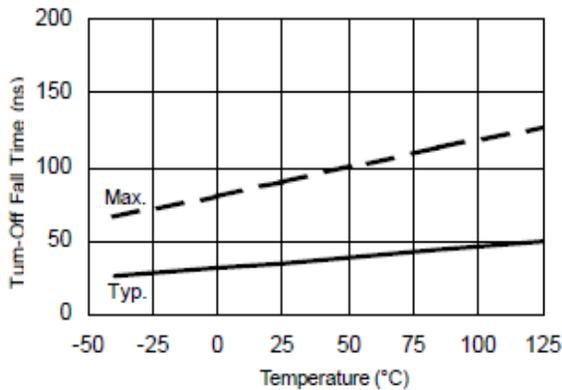
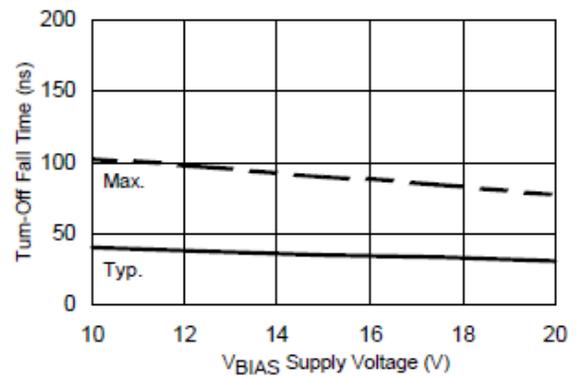
**Lead Definitions**

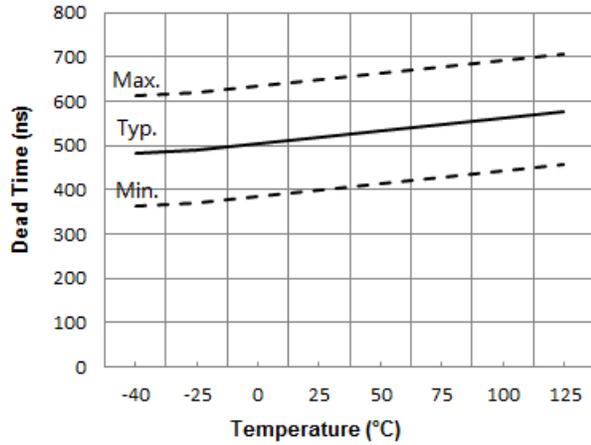
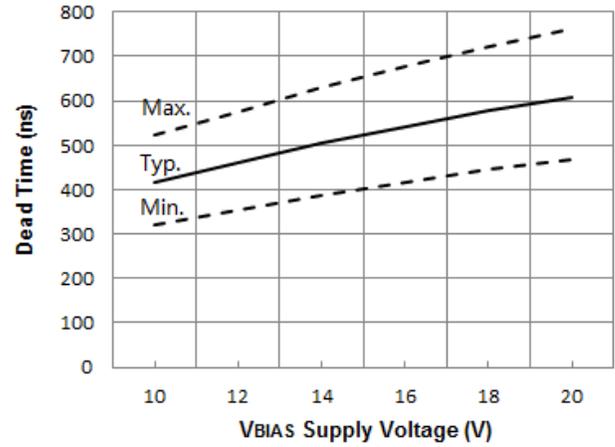
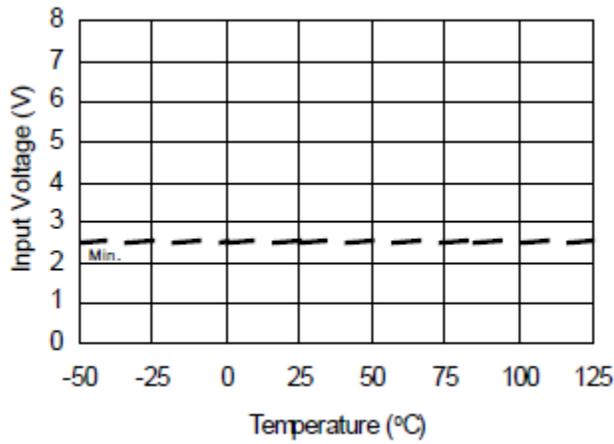
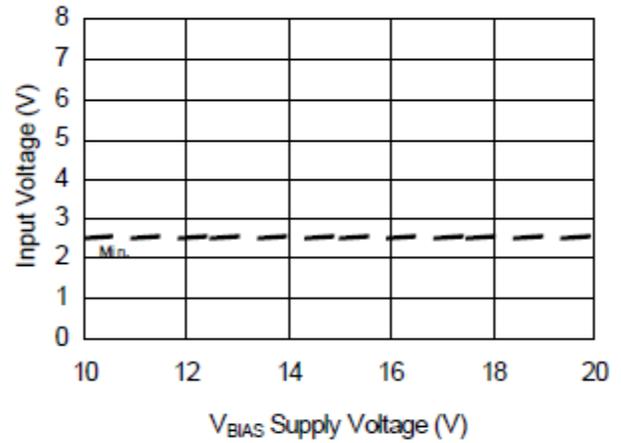
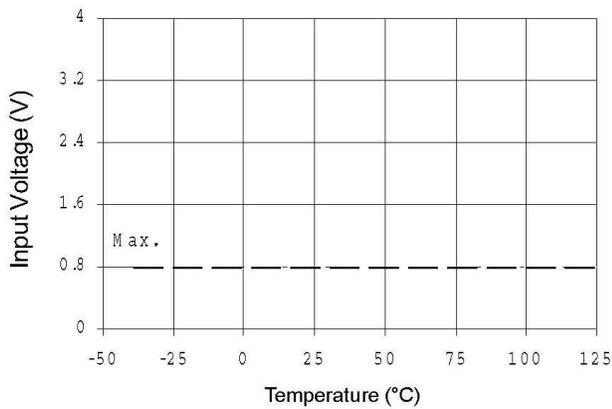
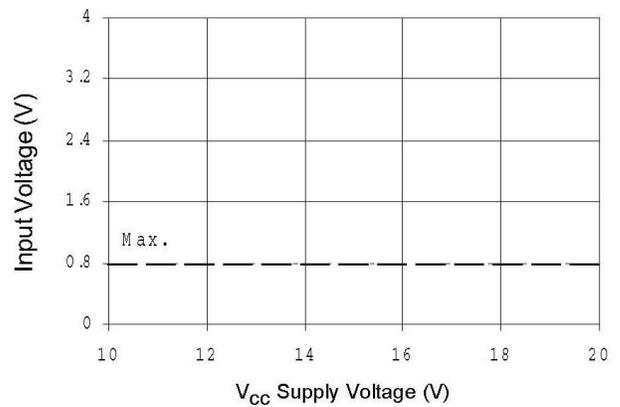
Symbol	Description
V <sub>CC</sub>	Low-side and logic supply voltage
V <sub>B</sub>	High-side gate drive floating supply
V <sub>S</sub>	High voltage floating supply return
IN	Logic inputs for high and low side gate driver output (HO and LO), in phase with HO
$\overline{SD}$	Logic inputs for shutdown
HO	High-side driver output
LO	Low-side driver output
COM	Low-side gate drive return

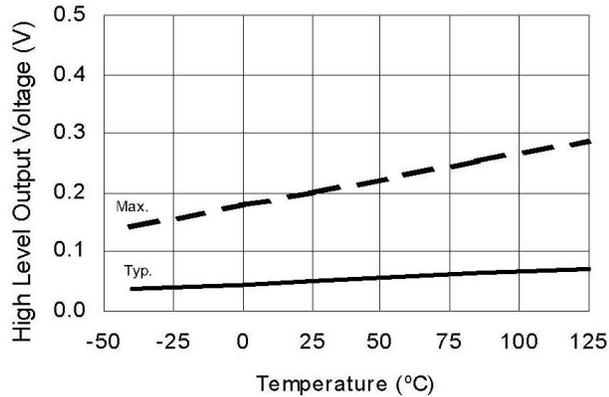
**Lead Assignments**


**Application Information and Additional Details**

**Figure 1. Input/Output Timing Diagram**

**Figure 2. Switching Time Waveform Definitions**

**Figure 3. Shutdown Waveform Definitions**

**Figure 4. Deadtime Waveform Definitions**

**Figure 5. Delay Matching Waveform Definitions**

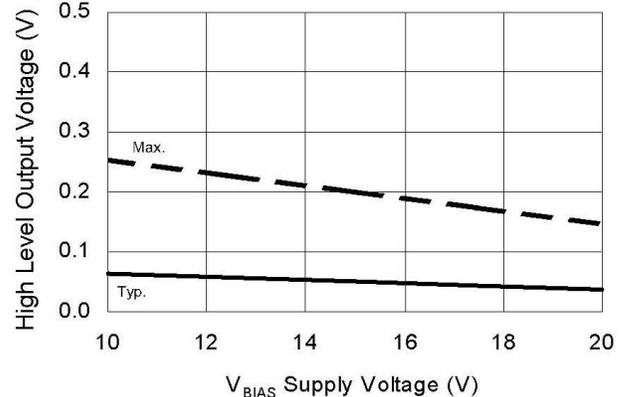
**Parameters trend with different temperature and voltage bias. (Fig.6 ~ Fig.25)**

**Figure 6A. Turn-On Time vs. Temperature**

**Figure 6B. Turn-On Time vs. Supply Voltage**

**Figure 6C. Turn-On Time vs. Input Voltage**

**Figure 7A. Turn-Off Time vs. Temperature**

**Figure 7B. Turn-Off Time vs. Supply Voltage**

**Figure 7C. Turn-Off Time vs. Input Voltage**


**Figure 8A. Shutdown Time vs. Temperature**

**Figure 8B. Shutdown Time vs. Supply Voltage**

**Figure 9A. Turn-On Rise Time vs. Temperature**

**Figure 9B. Turn-On Rise Time vs. Supply Voltage**

**Figure 10A. Turn-Off Fall Time vs. Temperature**

**Figure 10B. Turn-Off Fall Time vs. Supply Voltage**

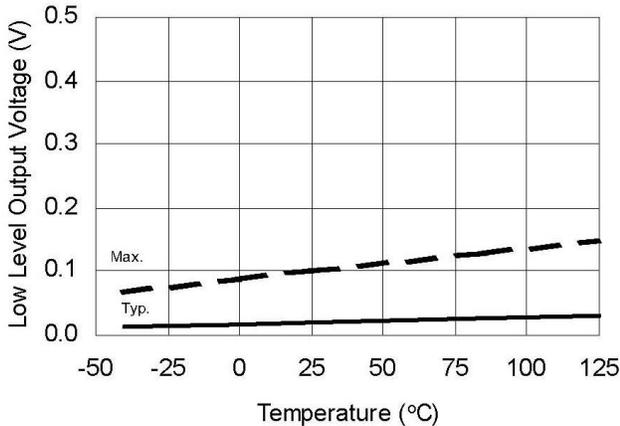

**Figure 11A. Deadtime vs. Temperature**

**Figure 11B. Deadtime vs. Supply Voltage**

**Figure 12A. Logic "1"(HO) & Logic "0"(LO) vs. Temperature**

**Figure 12B. Logic "1"(HO) & Logic "0"(LO) vs. Supply Voltage**

**Figure 13A. Logic "0"(HO) & Logic "1"(LO) vs. Temperature**

**Figure 13B. Logic "0"(HO) & Logic "1"(LO) vs. Supply Voltage**



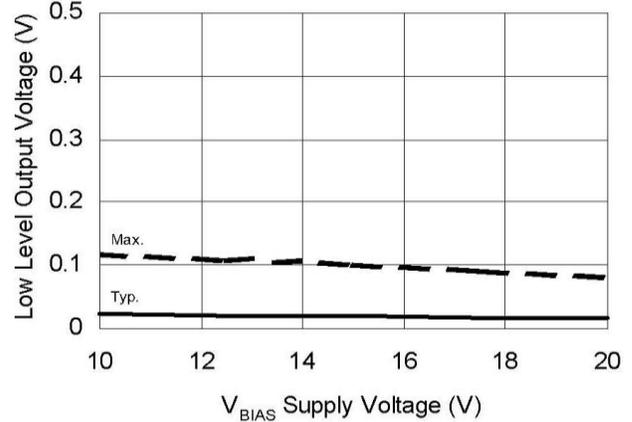
**Figure 14A. High Level Output Voltage vs. Temperature**



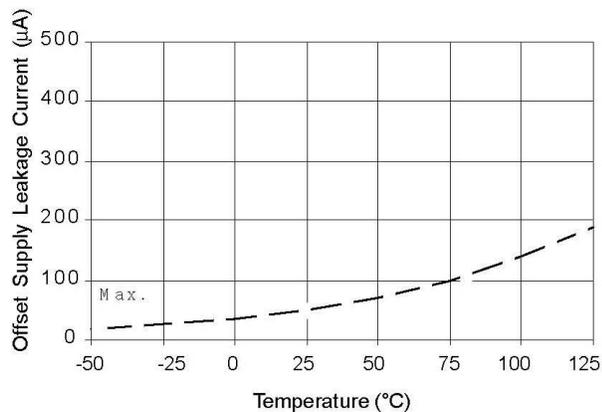
**Figure 14B. High Level Output Voltage vs. Supply Voltage**



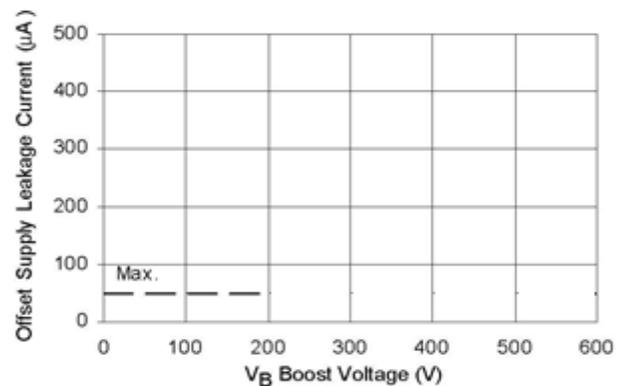
**Figure 15A. Low Level Output Voltage vs. Temperature**



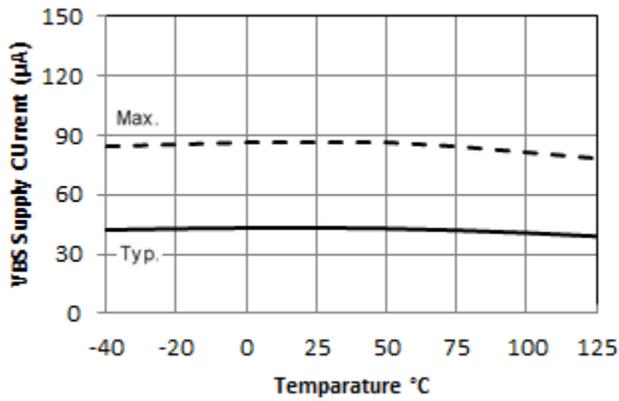
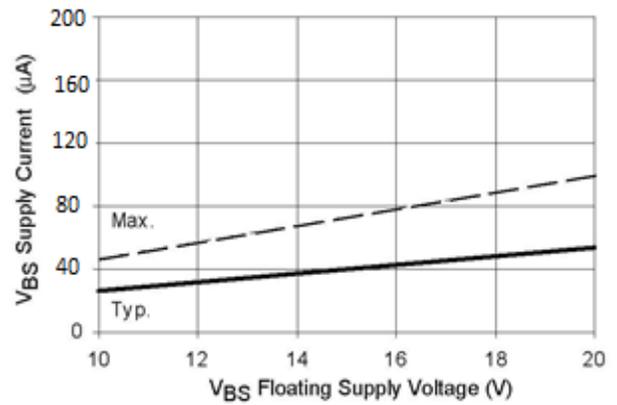
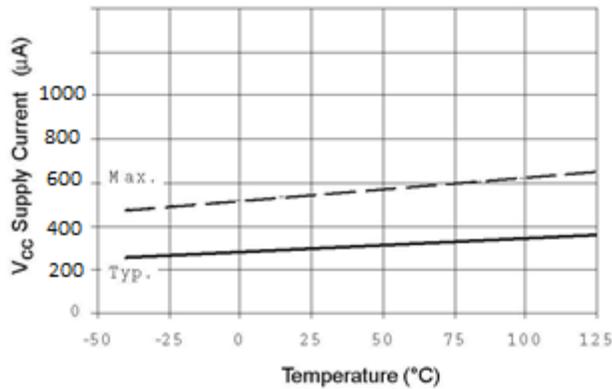
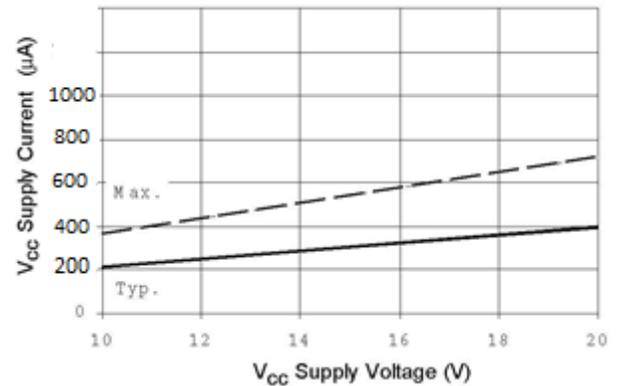
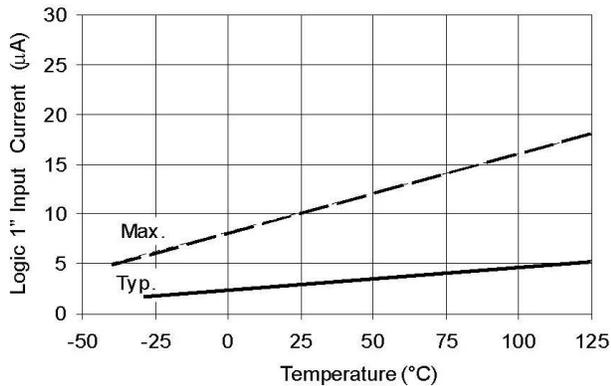
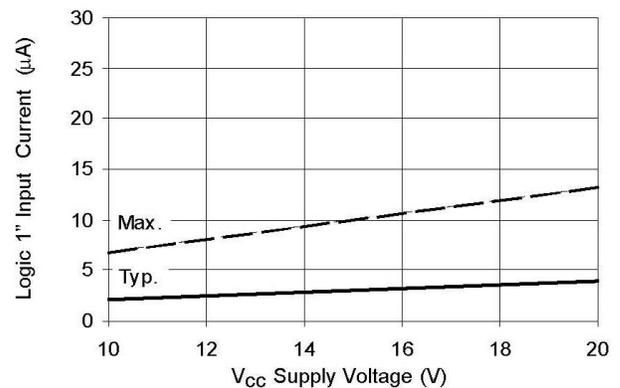
**Figure 15B. Low Level Output Voltage vs. Supply Voltage**

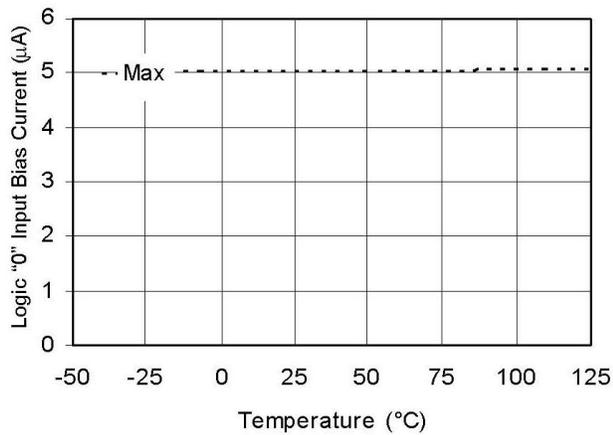


**Figure 16A. Offset Supply Current vs. Temperature**

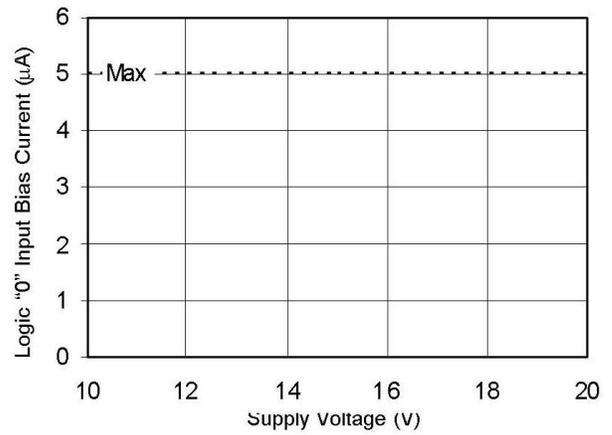


**Figure 16B. Offset Supply Current vs. offset Voltage**

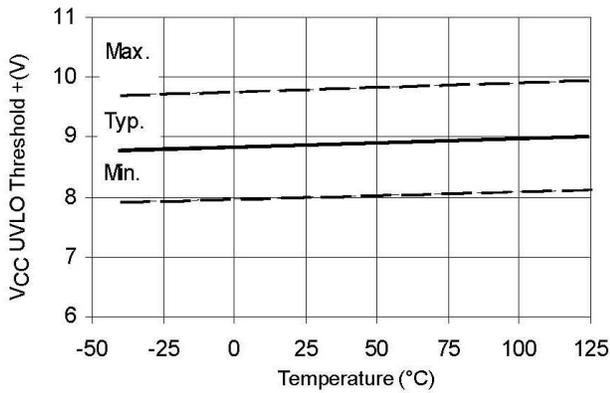

**Figure 17A.  $V_{BS}$  Supply Current vs. Temperature**

**Figure 17B.  $V_{BS}$  Supply Current vs. Supply Voltage**

**Figure 18A.  $V_{CC}$  Supply Current vs. Temperature**

**Figure 18B.  $V_{CC}$  Supply Current vs. Supply Voltage**

**Figure 19A. Logic "1" Input Current vs. Temperature**

**Figure 19B. Logic "1" Input Current vs. Supply Voltage**



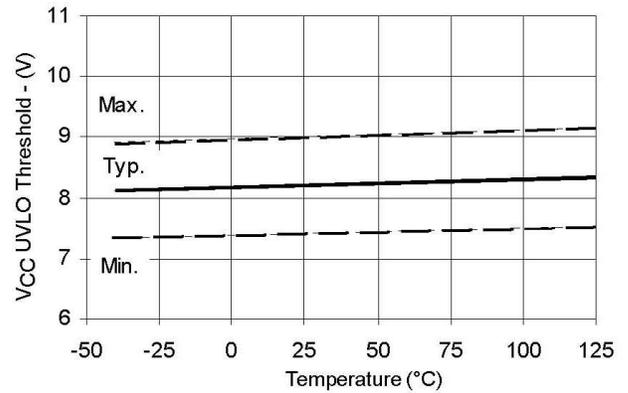
**Figure 20A. Logic "0" Input Bias Current vs. Temperature**



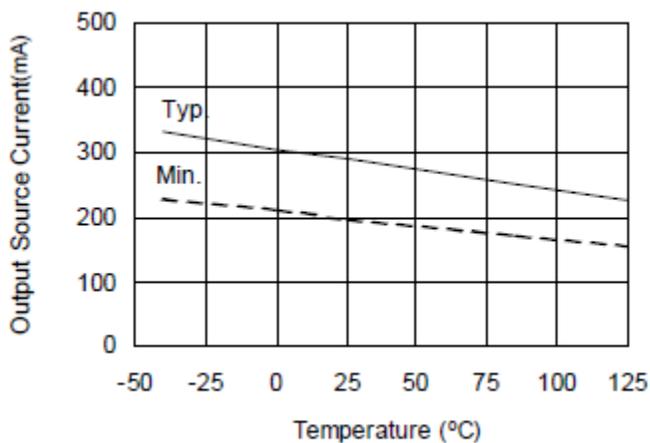
**Figure 20B. Logic "0" Input Current vs. Supply Voltage**



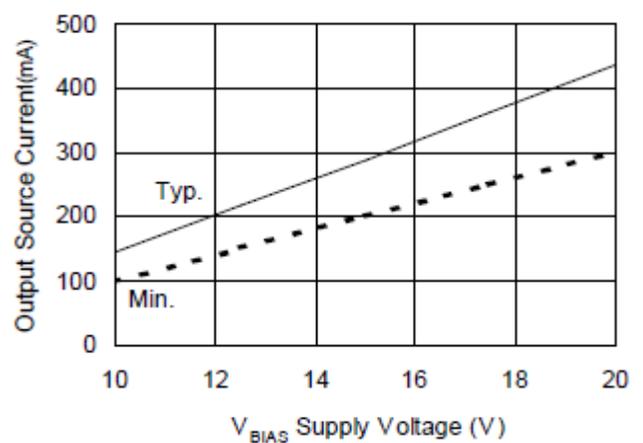
**Figure 21A.  $V_{CC}/V_{BS}$  Undervoltage Threshold(+) vs. Temperature**



**Figure 21B.  $V_{CC}/V_{BS}$  Undervoltage Threshold(-) vs. Temperature**



**Figure 22A. Output Source Current vs. Temperature**



**Figure 22B. Output Source Current vs. Supply Voltage**

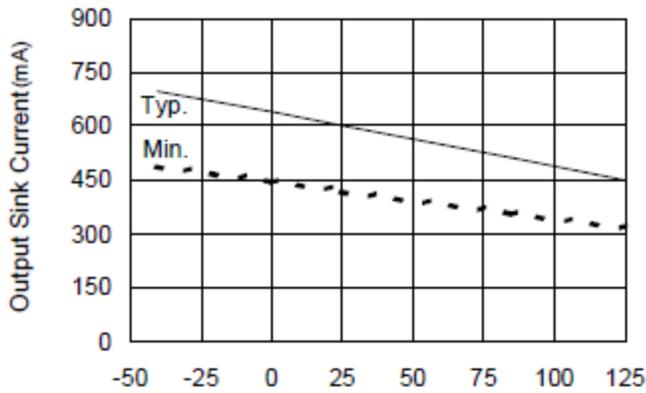


Figure 23A. Output Sink Current vs. Temperature

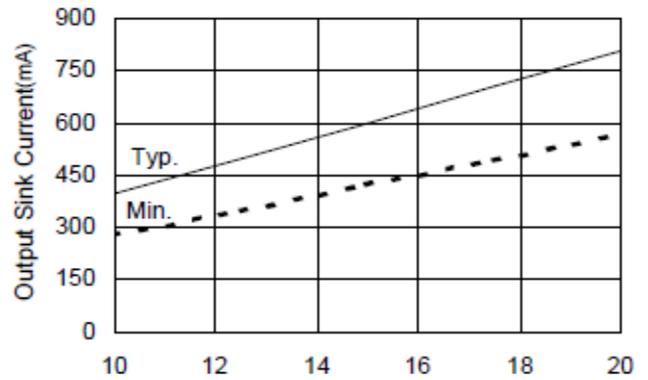


Figure 23B. Output Sink Current vs. Supply Voltage

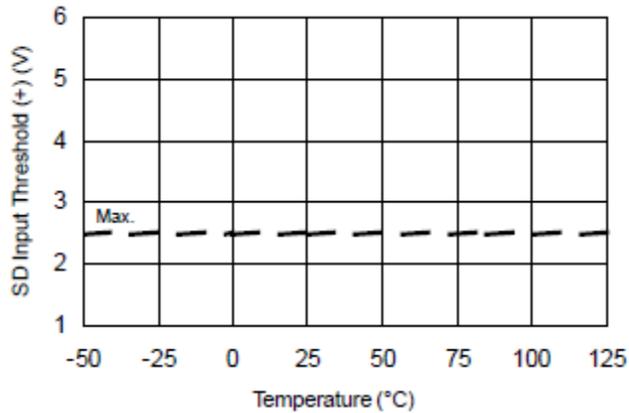


Figure 24A. SD input Positive Going Threshold(+) vs. Temperature

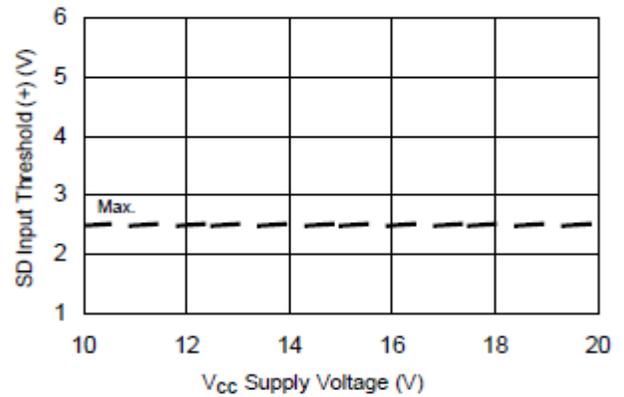


Figure 24B. SD input Positive Going Threshold(+) vs. Supply Voltage

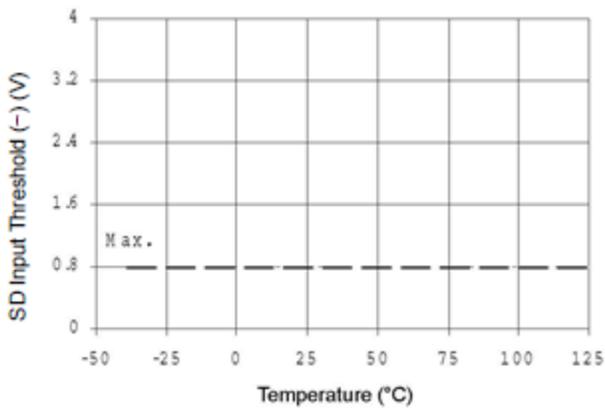


Figure 25A. SD input Negative Going Threshold(-) vs. Temperature

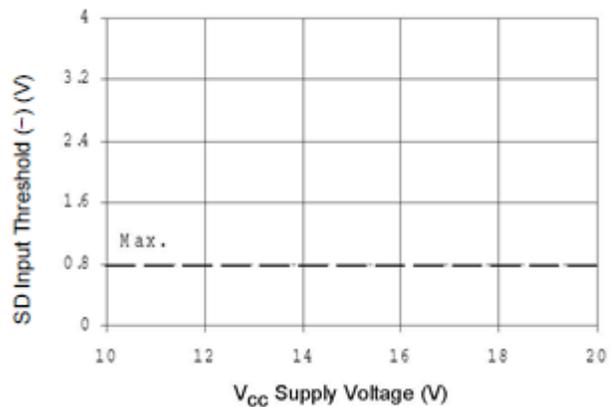
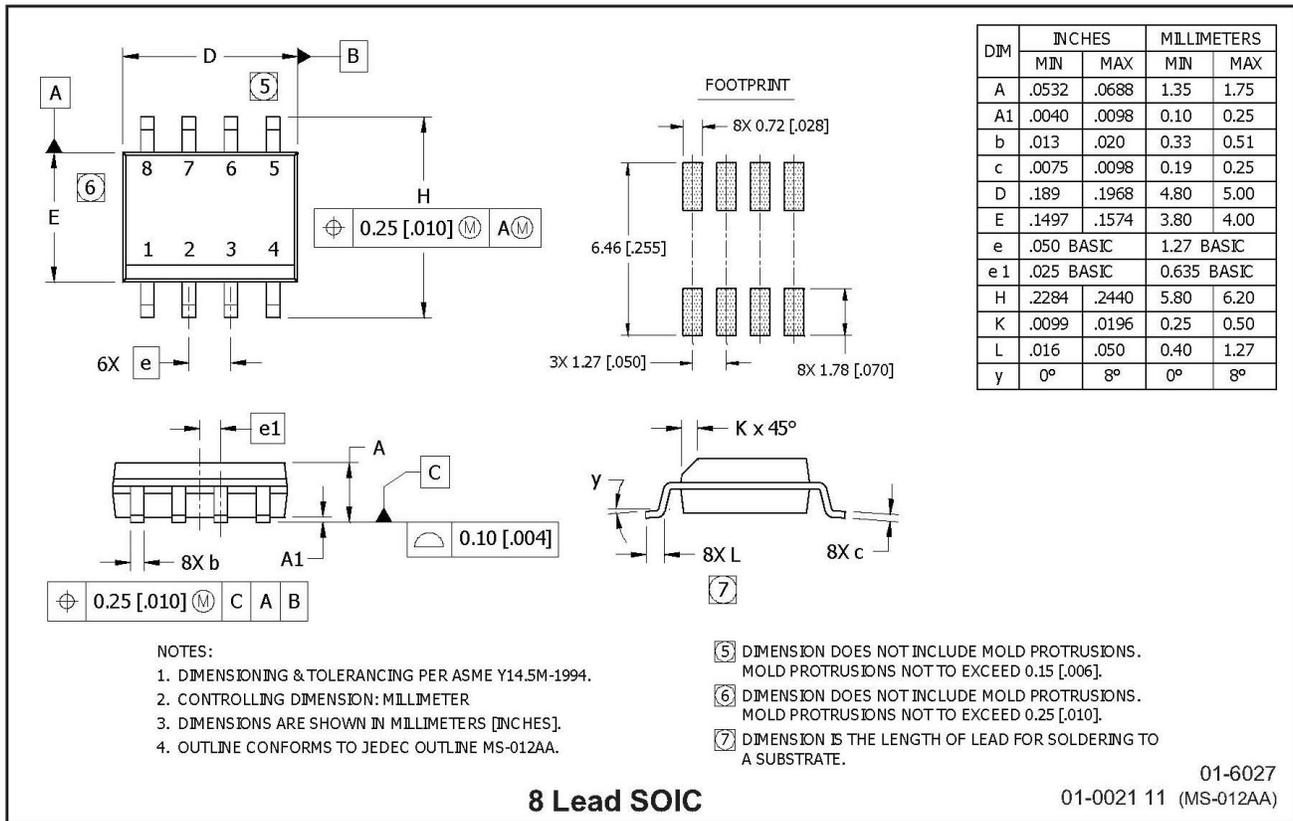
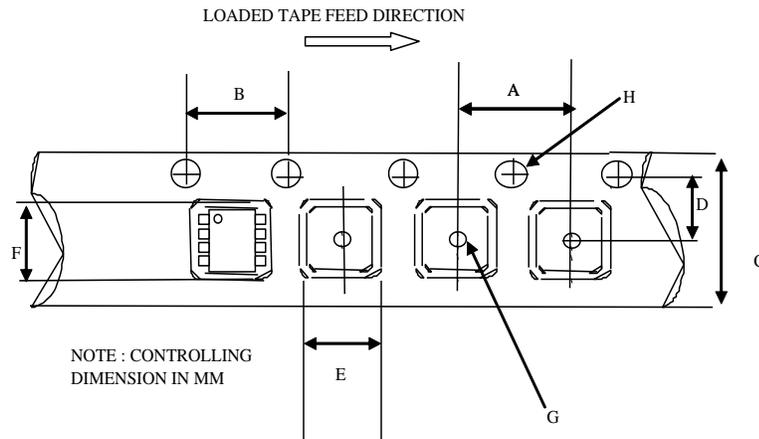


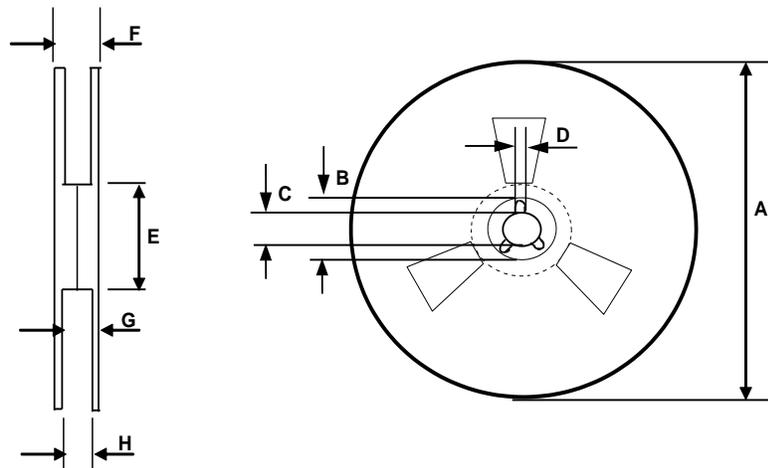
Figure 25B. SD input Negative Going Threshold(-) vs. Supply Voltage

## Package Details: 8-Lead SOIC



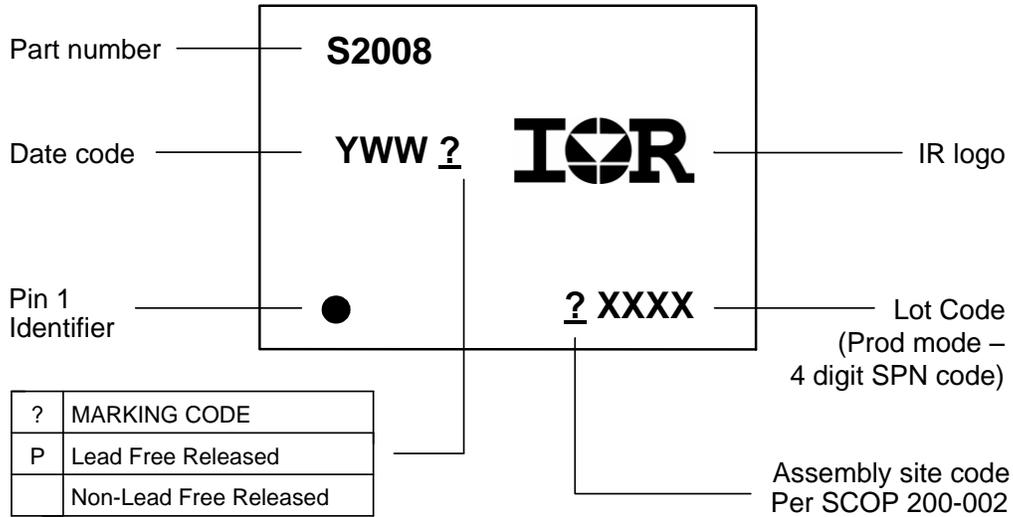
**Tape and Reel Details: 8-Lead SOIC**

**CARRIER TAPE DIMENSION FOR 8SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062


**REEL DIMENSIONS FOR 8SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information**



**8-Lead SOIC8  
IRS2008SPBF**

**Qualification Information**

<b>Qualification Level</b>		Industrial <sup>†</sup>	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>		8 Lead SOIC	MSL2 <sup>††</sup> , 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)	
	Machine Model	Class A (per EIA/JEDEC standard EIA/JESD22-A115)	
<b>IC Latch-Up Test</b>		Class II, Level A (per JESD78)	
<b>RoHS Compliant</b>		Yes	

- † Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
- †† Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

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